

# PMV56XN

$\mu$ TrenchMOS™ extremely low level FET

Rev. 01 — 26 February 2003

Product data

## 1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMV56XN in SOT23.

## 2. Features

- TrenchMOS™ technology
- Very fast switching
- Low threshold voltage
- Subminiature surface mount package.

## 3. Applications

- Battery management
- High-speed switch
- Low power DC-to-DC converter.

## 4. Pinning information

Table 1: Pinning - SOT23, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view MSB003</p> <p><b>SOT23</b></p>	<p>MBB076</p>
2	source (s)		
3	drain (d)		

## 5. Quick reference data

**Table 2: Quick reference data**

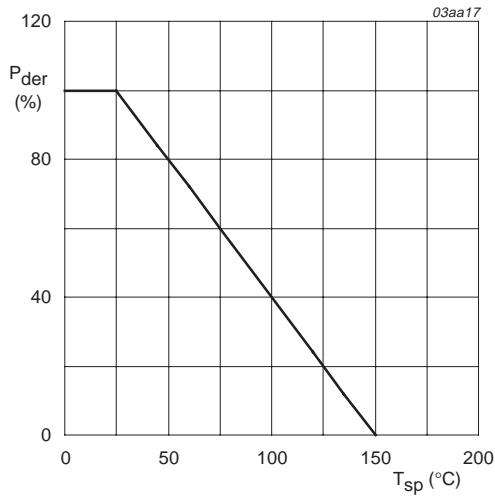
Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 4.5\text{ V}$	-	2.5	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$	-	0.83	W
$T_j$	junction temperature		-	150	°C
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 3.6\text{ A}; T_j = 25\text{ °C}$	56	85	m $\Omega$
		$V_{GS} = 2.5\text{ V}; I_D = 3.1\text{ A}; T_j = 25\text{ °C}$	77	115	m $\Omega$

## 6. Limiting values

**Table 3: Limiting values**

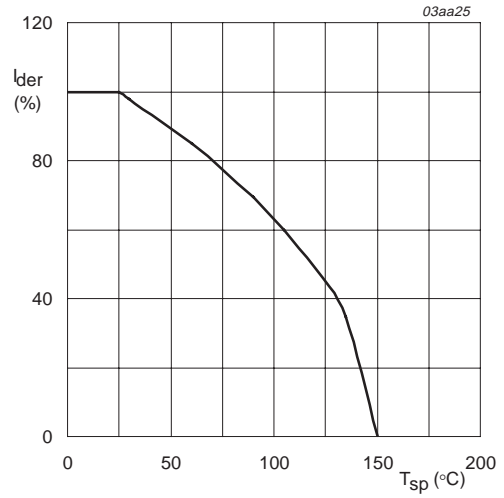
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
$V_{GS}$	gate-source voltage (DC)		-	$\pm 8$	V
$I_D$	drain current (DC)	$T_{sp} = 25\text{ °C}; V_{GS} = 4.5\text{ V};$ <b>Figure 2 and 3</b>	-	2.5	A
		$T_{sp} = 70\text{ °C}; V_{GS} = 4.5\text{ V};$ <b>Figure 2</b>	-	2	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ <b>Figure 3</b>	-	10.9	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C};$ <b>Figure 1</b>	-	0.83	W
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-65	+150	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{sp} = 25\text{ °C}$	-	0.7	A



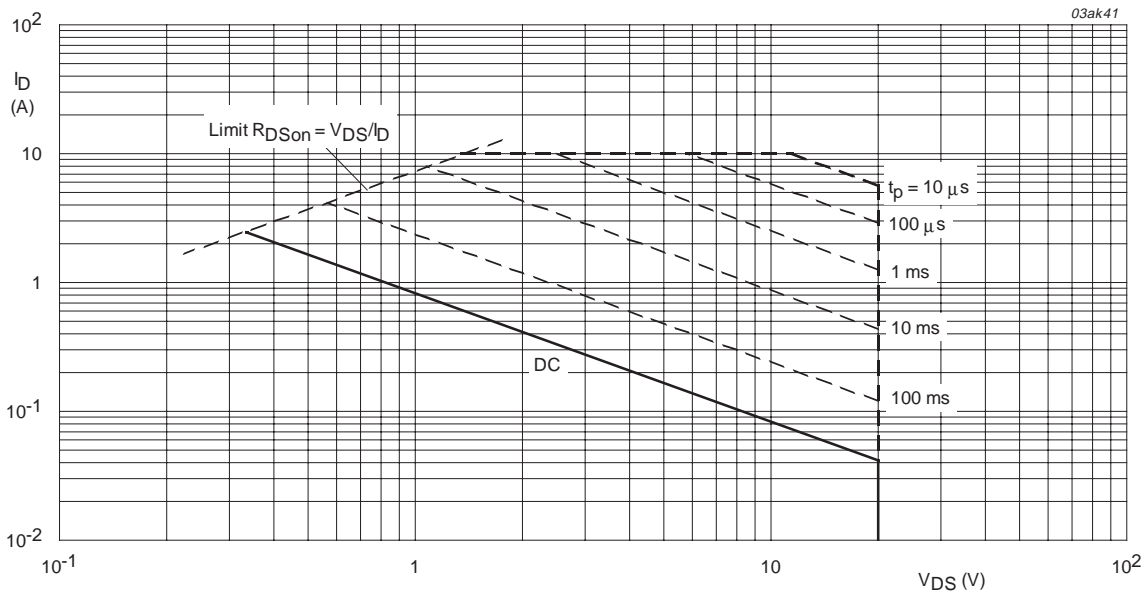
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse;  $V_{GS} = 4.5 V$ .

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	150	K/W

### 7.1 Transient thermal impedance

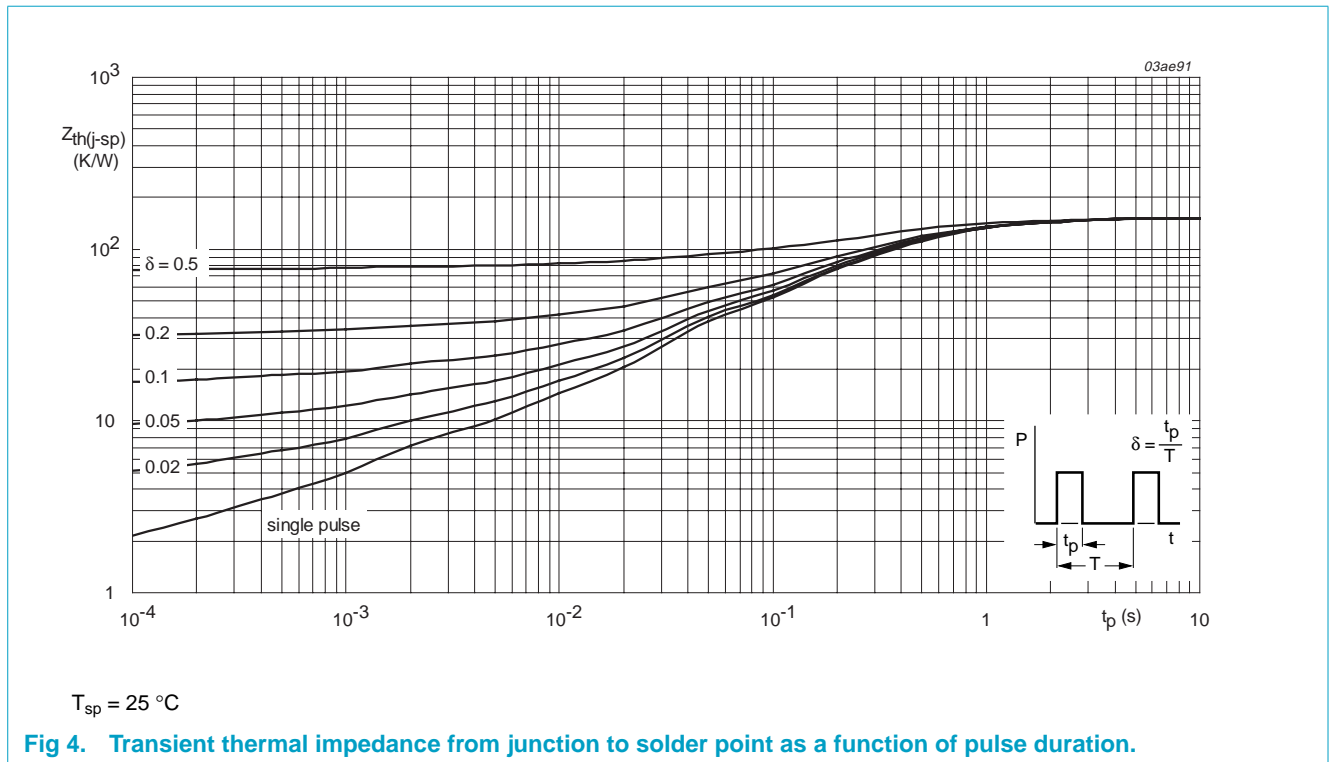


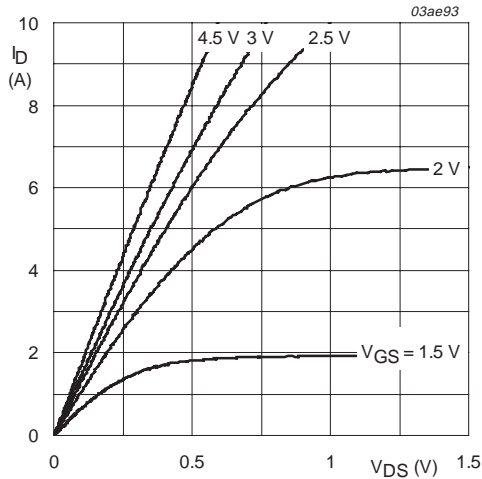
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration.

## 8. Characteristics

**Table 5: Characteristics**

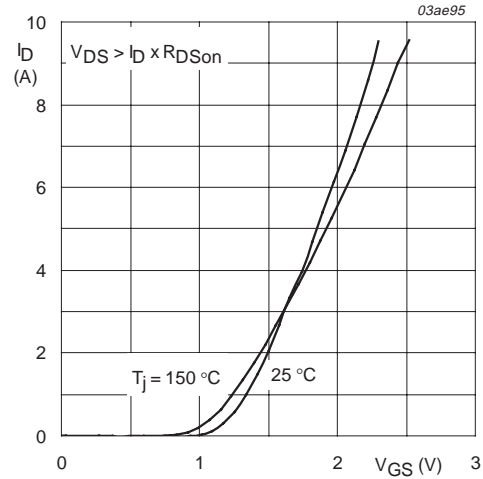
$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}; V_{GS} = 0\text{ V}$	20	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$ ; <b>Figure 9</b>	0.65	-	-	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$	-	0.01	1.0	$\mu\text{A}$
			-	-	10	$\mu\text{A}$
			-	-	-	-
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 8\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 3.6\text{ A}$ ; <b>Figure 7 and 8</b>	-	56	85	$\text{m}\Omega$
		$V_{GS} = 2.5\text{ V}; I_D = 3.1\text{ A}$ ; <b>Figure 7 and 8</b>	-	77	115	$\text{m}\Omega$
<b>Dynamic characteristics</b>						
$Q_{g(tot)}$	total gate charge	$V_{DD} = 10\text{ V}; V_{GS} = 4.5\text{ V}; I_D = 3.6\text{ A}$ ; <b>Figure 13</b>	-	5.4	-	nC
$Q_{gs}$	gate-source charge		-	0.65	-	nC
$Q_{gd}$	gate-drain (Miller) charge		-	1.6	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 10\text{ V}; f = 1\text{ MHz}$ ; <b>Figure 11</b>	-	230	-	pF
$C_{oss}$	output capacitance		-	125	-	pF
$C_{rss}$	reverse transfer capacitance		-	80	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\text{ V}; R_L = 5.5\text{ }\Omega; V_{GS} = 4.5\text{ V}; R_G = 6\text{ }\Omega$	-	12	-	ns
$t_r$	rise time		-	23	-	ns
$t_{d(off)}$	turn-off delay time		-	50	-	ns
$t_f$	fall time		-	34	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 1.6\text{ A}; V_{GS} = 0\text{ V}$ ; <b>Figure 12</b>	-	0.8	1.2	V



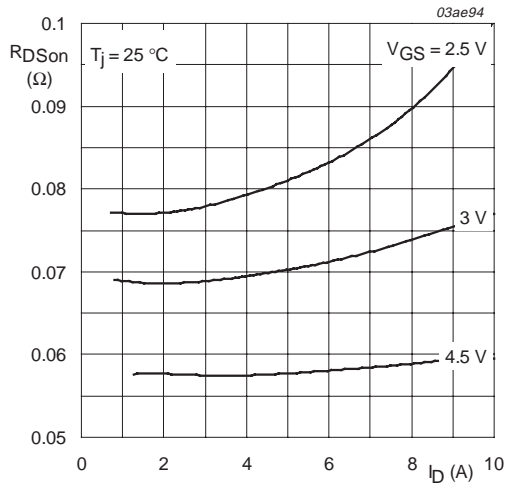
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



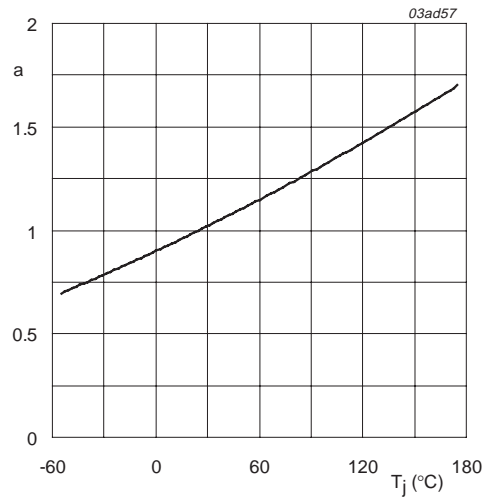
$T_j = 25\text{ °C}$  and  $150\text{ °C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



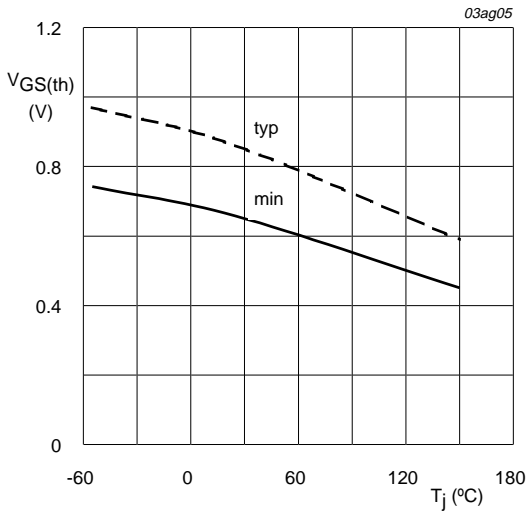
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



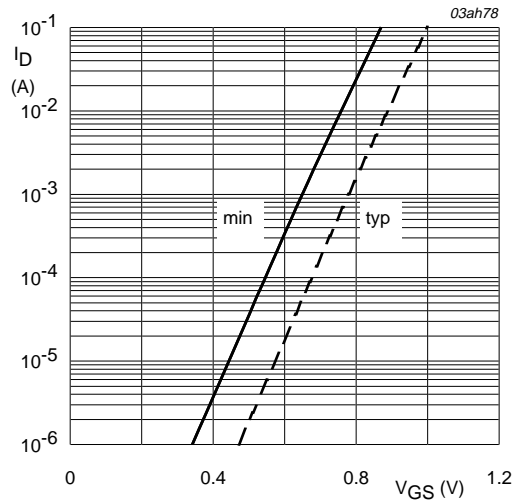
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



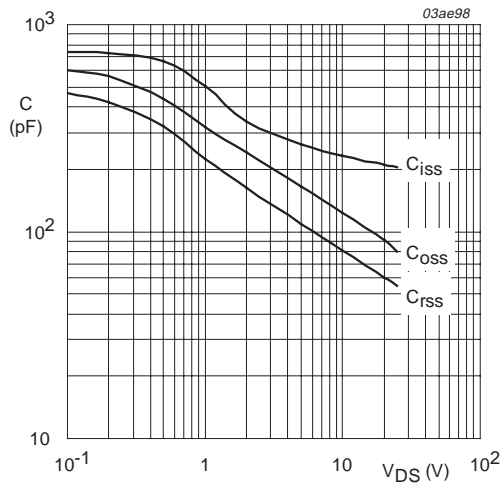
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



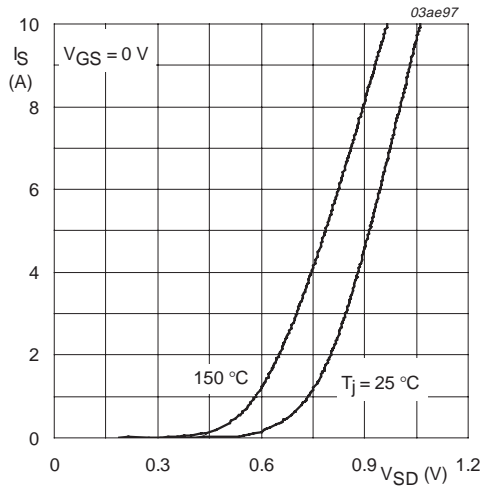
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



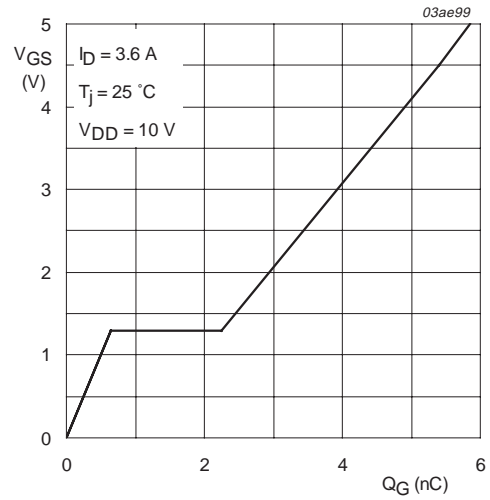
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 3.6\text{ A}$ ;  $V_{DD} = 10\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**



9. Package outline

Plastic surface mounted package; 3 leads

SOT23

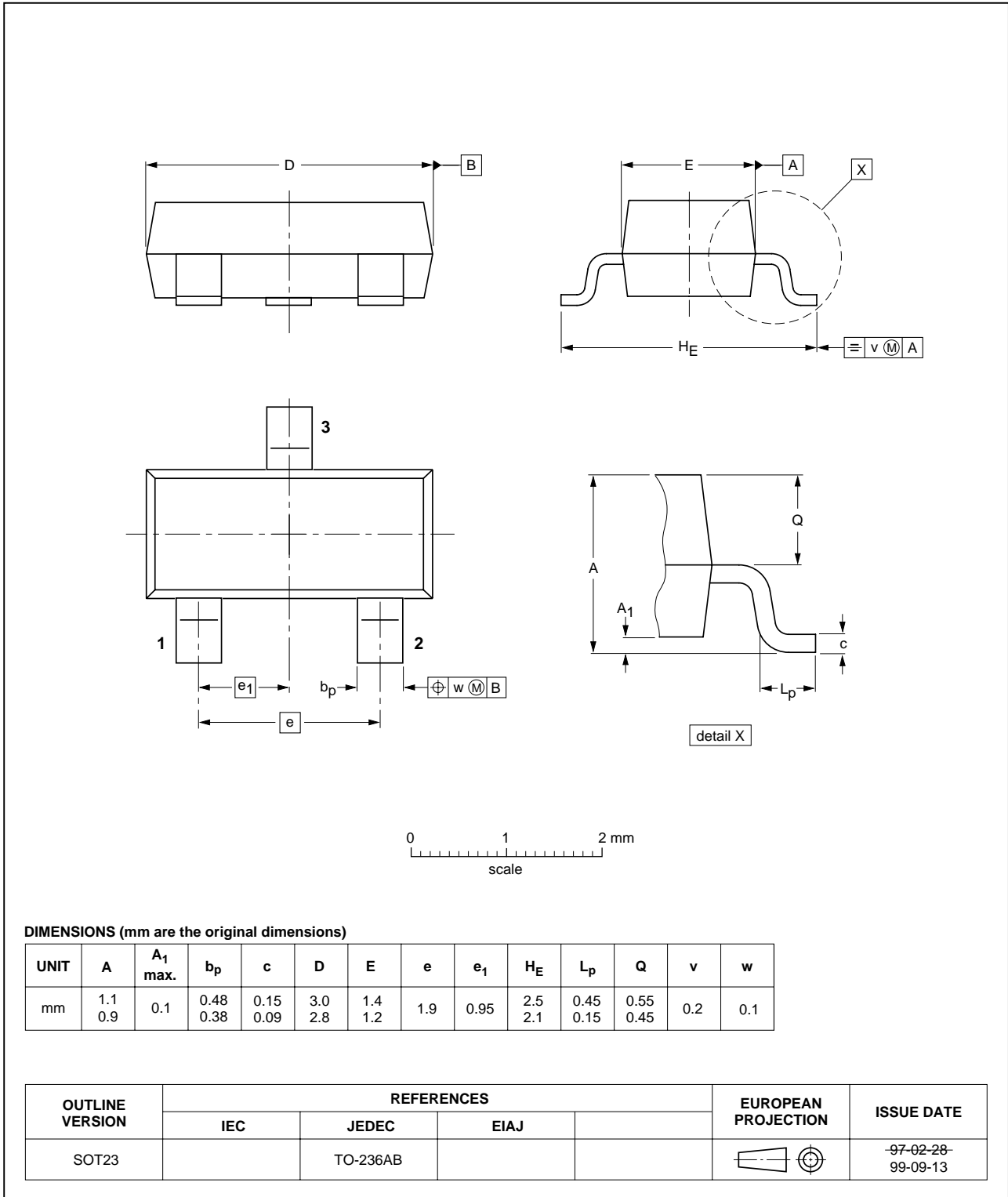


Fig 14. SOT23.

## 10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20030226	-	Product data (9397 750 11096).

## 11. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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For sales office addresses, send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

Fax: +31 40 27 24825

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